IDEC Chip Design Contest

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A 4 – 8 GHz CMOS LNA at Operating at Cryogenic Temperatures

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Introduction

Low-noise amplifiers (LNAs) for quantum computing readout circuits typically operate in the 4–8 GHz frequency range, where qubit signals are processed. In cryogenic environments, the signal level is extremely small, making the noise performance of the LNA a critical factor in overall system sensitivity. In this work, a CMOS-based LNA is proposed to achieve low-noise performance while maintaining compatibility with scalable integration. To realize wideband operation over the target frequency range, a parallelized matching structure derived from a series RLC network is employed. This approach enables broadband impedance matching, overcoming the limitations of conventional narrowband designs. As a result, the proposed architecture is suitable for quantum readout applications requiring both low noise and wideband characteristics.

Circuit Design

The proposed LNA adopts a fully differential architecture, allowing low-noise performance even in a CMOS implementation. The differential structure effectively suppresses common-mode noise and improves signal integrity, which is essential for amplifying weak qubit readout signals. The amplifier consists of a three-stage topology, where one stage incorporates a series RLC network configured in parallel to achieve broadband matching. This design enables stable operation across the 4–8 GHz bandwidth. The implemented LNA achieves approximately 20 dB gain, a 4–8 GHz bandwidth, and a noise temperature of about 2 K, demonstrating its suitability for cryogenic quantum readout systems.

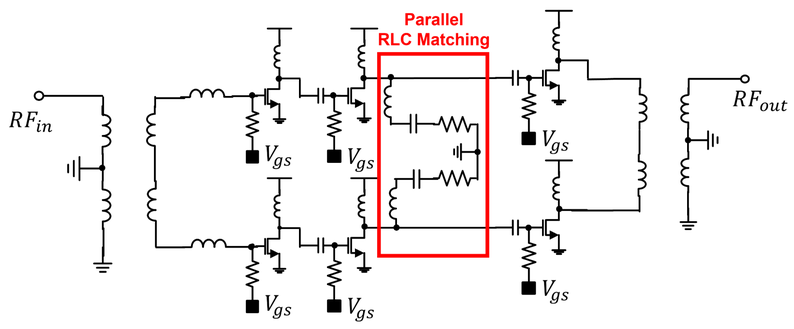

Fig 1 .LNA Schematic.

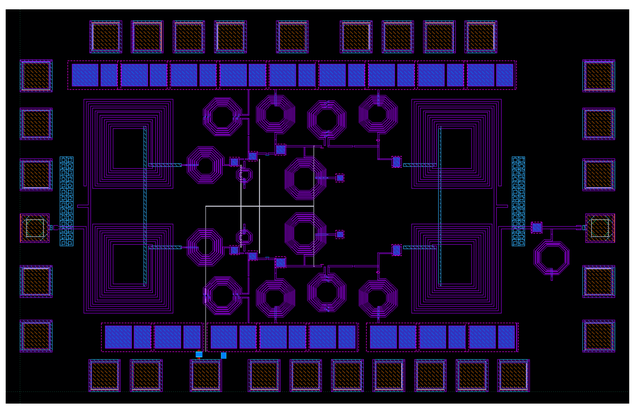

Fig 2 . Fabricated LNA.

Results

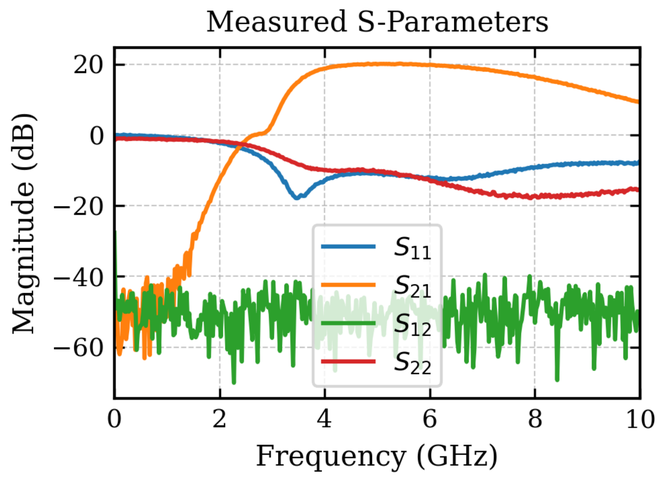

Fig 3 . S-parameters results of the LNA.

- **This chip is fabricated Samsung 28 - nm CMOS process.**
- **The bandwidth is 4 GHz to 8 GHz.**
- **Gain is 20 dB with 15mW power consumption.**
- **Noise is 2K at 4K temperature.**

Cryogenic LNA Comparison Table					
Ref.	**Tech.**	**Gain (dB)**	**Bandwidth (GHz)**	**Noise (K)**	**Power (mW)**
[1]	**65nm CMOS**	**38**	**3.9 – 5.3**	**10.2**	**23.1**
[2]	**22nm FDSOI**	**37**	**5 – 6**	**4.4**	**15.8**
[3]	**180nm CMOS**	**15**	**5 – 6**	**1.8**	**14.78**
This Work	**28nm CMOS**	**20**	**4 – 8**	**2**	**15**

[1] S. Das, S. Raman, and J. C. Bardin, "Design and Implementation of a 3.9-to-5.3 GHz 65 nm Cryo-CMOS LNA with an Average Noise Temperature of 10.2 K," *IEEE MTT-S International Microwave Symposium*, 2022.

[2] S. Das, S. Raman, and J. C. Bardin, "A 4-to-6-GHz Cryogenic CMOS LNA With 4.4-K Average Noise Temperature in 22-nm FDSOI," *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 4, pp. 411–414, Apr. 2024.

[3] C. Zheng *et al*., "A 5.8GHz Band LNA in TSMC 0.18μm CMOS Technology," *2024 4th International Conference on Electronics, Circuits and Information Engineering*, 2024.

Conclusion

In this work, a CMOS-based LNA targeting the 4–8 GHz band for quantum computing readout applications has been presented. By employing a differential architecture, low-noise performance was achieved, while the use of a parallelized series RLC matching network enabled broadband operation. The proposed design demonstrates approximately 20 dB gain, 4–8 GHz bandwidth, and 2 K noise temperature, confirming its effectiveness for cryogenic low-noise amplification in quantum systems.